600V Half-Bridge Driver

1. Description

The IR2104S is a high voltage, high speed power MOSFET and IGBT drivers with dependent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 600 V.

2. Features

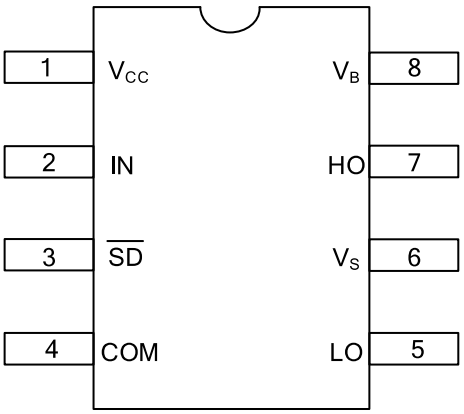
- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout
- 3.3 V, 5 V, and 15 V logic compatible
- Cross-conduction prevention logic
- Matched propagation delay for both channels
- Internal set deadtime
- Shutdown input turns off both channels
- RoHS compliant
- SOIC-8 and PDIP-8 package

3. Ordering Information

Type Number	Package Type	Packing
IR2104S	SOIC-8	Tape & Reel
IR2104	DIP-8	Tube

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

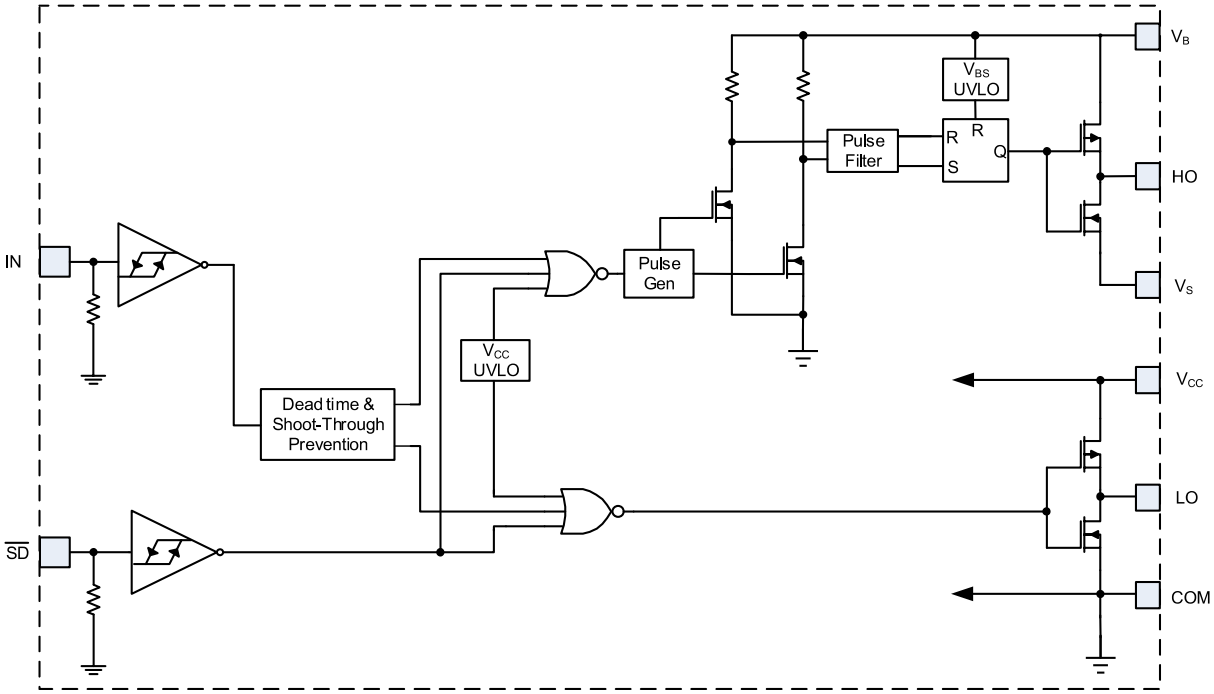
4. Pin Configuration



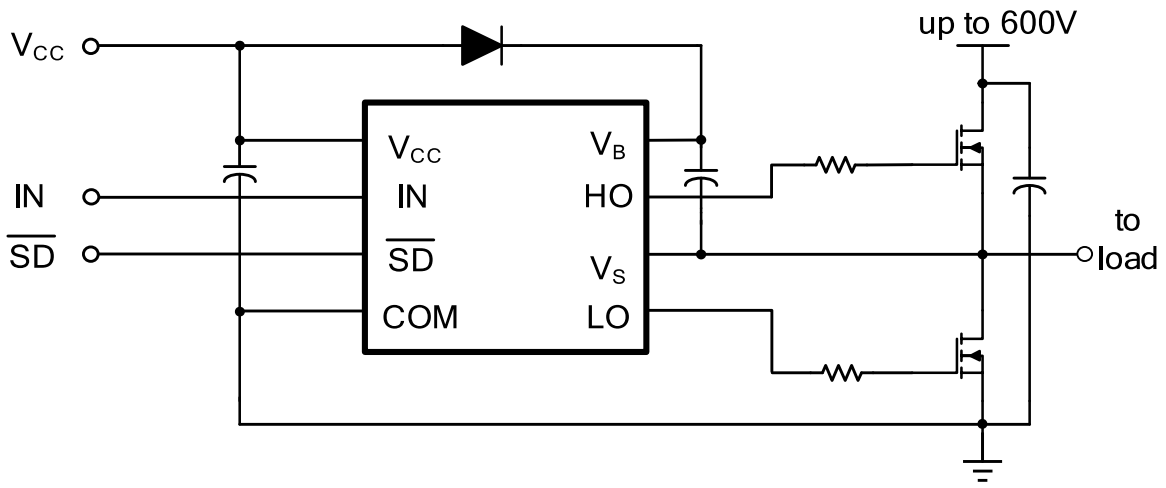
5. Pin Description

No.	Pin	Description
1	V_{CC}	Low-side and logic fixed supply
2	IN	Logic input for high-side and low-side gate driver outputs (HO and LO), in phase with HO
3	$\overline{SD}$	Logic input for shutdown
4	COM	Low-side return
5	LO	Low-side gate drive output
6	V_S	High-side floating supply return
7	HO	High-side gate drive output
8	V_B	High-side floating supply

6. Functional Block Diagram



7. Typical Application Circuit



(Refer to Lead Assignments for correct configuration). This diagram shows electrical connections only. Please refer to our Application Notes and DesignTips for proper circuit board layout.

8. DYNAMIC ELECTRICAL CHARACTERISTICS

V_{BIAS} (V_{CC}, V_{BS}) = 15 V, C_L = 1000 pF and T_A = 25°C unless otherwise specified.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{on}	Turn-on propagation delay	V_S = 0 V	---	680	820	ns
t_{off}	Turn-off propagation delay	V_S = 600 V	---	150	220	
t_{sd}	Shutdown propagation delay		---	160	220	
t_r	Turn-on rise time		---	70	170	
t_f	Turn-off fall time		---	35	90	
DT	Deadtime, LS turn-off to HS turn-on & HS turn-on to LS turn-off		400	520	650	
MT	Delay matching, HS & LS turn-on/off		---	---	60	

9. STATIC ELECTRICAL CHARACTERISTICS

V_{BIAS} (V_{CC}, V_{BS}) = 15 V and T_A = 25°C unless otherwise specified. The V_{IN}, V_{TH}, and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IH}	Logic “1” input voltage	V_{CC} = 10 V to 20V	2.5	---	---	V
V_{IL}	Logic “0” input voltage		---	---	0.8	
$V_{SD, TH+}$	SD input positive going threshold		2.5	---	---	
$V_{SD, TH-}$	SD input negative going threshold		---	---	0.8	
V_{OH}	High level output voltage, V_{BIAS} - V_O	I_O = 2 mA	---	0.05	0.2	
V_{OL}	Low level output voltage, VO		---	0.02	0.1	
I_{LK}	Offset supply leakage current	V_B = V_S = 600 V	---	---	50	μA
I_{QBS}	Quiescent V_{BS} supply current	V_{IN} = 0 V or 5 V	---	60	75	
I_{QCC}	Quiescent $_{VCC}$ supply current		---	170	270	
I_{IN+}	Logic “1” input bias current	V_{IN} = 5 V	---	3	10	
I_{IN-}	Logic “0” input bias current	V_{IN} = 0 V	---	---	5	
V_{CCUV+} V_{BSUV+}	V_{CC} & V_{BS} supply undervoltage positive going threshold		8	8.9	9.8	V
V_{CCUV-} V_{BSUV-}	V_{CC} & V_{BS} supply undervoltage negative going threshold		7.4	8.2	9	
I_{O+}	Output high short circuit pulsed current	V_O = 0 V, V_{IN} = V_{IH} $P_W \leqslant$ 10 μs	130	290		mA
I_{O-}	Output low short circuit pulsed current	V_O = 15 V, V_{IN} = V_{IL} $P_W \leqslant$ 10 μs	270	600		

10. DETAILED INFORMATION

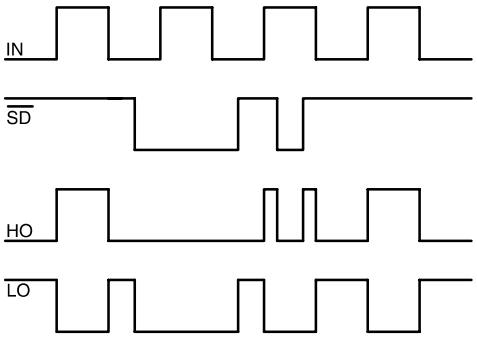


Figure 1. Input/Output Timing Diagram

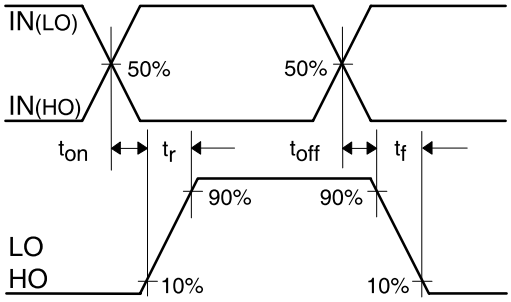


Figure 2. Switching Time Waveform Definitions

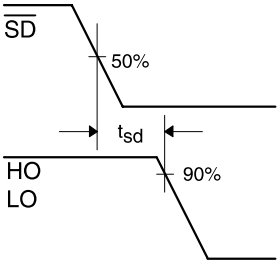


Figure 3. Shutdown Waveform Definitions

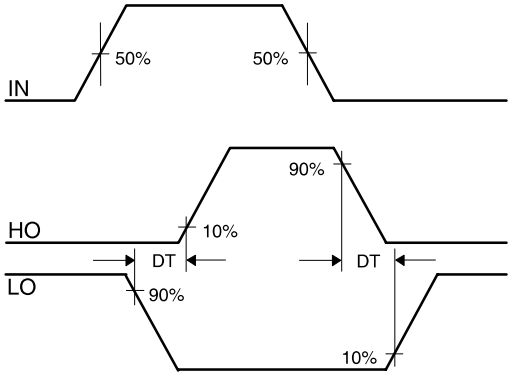


Figure 4. Deadtime Waveform Definitions

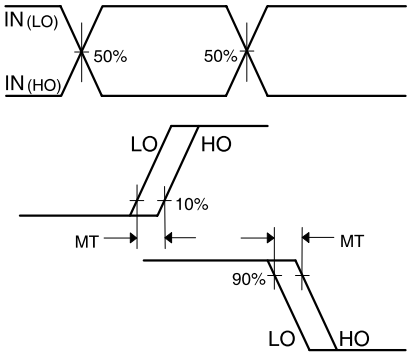
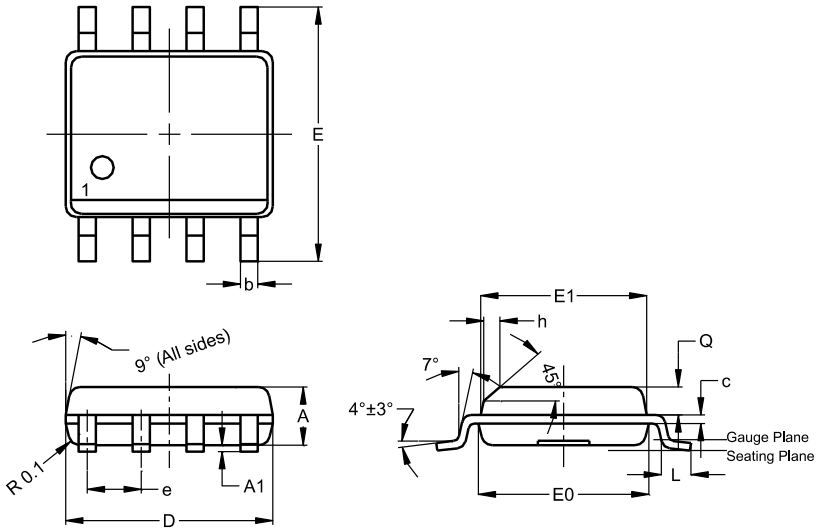


Figure 5. Delay Matching Waveform Definitions

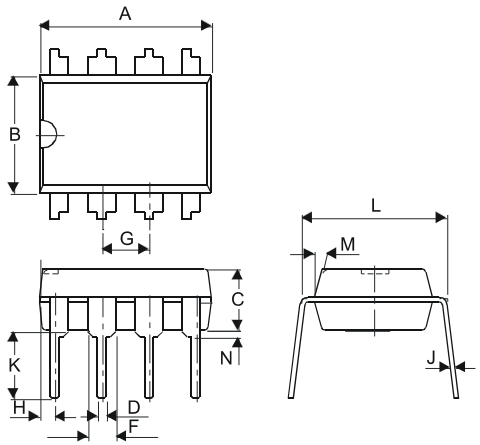
11. Package Outlines

SOIC-8



SOIC-8			
Dim	Min	Max	Typ
A	1.40	1.50	1.45
A1	0.10	0.20	0.15
b	0.30	0.50	0.40
c	0.15	0.25	0.20
D	4.85	4.95	4.90
E	5.90	6.10	6.00
E1	3.80	3.90	3.85
E0	3.85	3.95	3.90
e	--	--	1.27
h	-	--	0.35
L	0.62	0.82	0.72
Q	0.60	0.70	0.65
All Dimensions in mm			

DIP-8



PDIP-8		
Dim	Min	Max
A	9.02	9.53
B	6.15	6.35
C	3.10	3.50
D	0.36	0.56
F	1.40	1.65
G	2.54 typ.	
H	0.71	0.97
J	0.20	0.36
K	2.92	3.81
L	7.62	8.26
M	-	15°
N	0.38 (min)	
All Dimensions in mm		

12. Disclaimers

Limited warranty and liability

Information in this document is believed to be accurate and reliable. However, Fulihao does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. It is the customer's responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application.

Suitability for use

Fulihao products are designed for specific applications and should not be used for any purpose (including, without limitation, automotive, aerospace, medical, life-saving applications, or any other application which requires especially high reliability for the prevention of such defect as may directly cause damage to the third party's life, body or property) not expressly set forth in applicable Fulihao product documentation.

Right to make changes

Fulihao reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner. Fulihao takes no responsibility for the content in this document if provided by an information source outside of Fulihao. This document supersedes and replaces all information supplied prior to the publication hereof.